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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,825	01/05/2001	Iain Robertson	TI-28925	5403

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EXAMINER	
KADING, JOSHUA A	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,825	ROBERTSON ET AL.	
	Examiner	Art Unit	
	Joshua Kading	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10 and 15* is/are rejected.

7)☒ Claim(s) *8 and 11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by New (U.S. Patent 5,956,748).

Regarding claim 5, New discloses, "a method of transferring data words from a receive clock domain into a transmit clock domain, comprising the steps of:

applying a data word to an input of a buffer having a plurality of entries (figure 2, element 232);

responsive to a write valid bit associated with a first one of the plurality of entries indicating that the first one of the plurality of entries does not contain valid data, the first one of the plurality of entries indicated by a current value of a write pointer: storing the applied data word into the first one of the plurality of entries (figure 2, elements 203 and 205 as described in col. 4, lines 42-50);

setting the write valid bit associated with the first one of the plurality of entries (col. 4, lines 42-50 whereby enabling the write operation the write bit has been set); and

setting a read valid bit associated with the first one of the plurality of entries (col. 5, lines 18-25 whereby enabling the read operation the read bit has been set); and

responsive to a read valid bit associated with a second one of the plurality of entries indicating that a second one of the plurality of entries contains valid data, the second one of the plurality of entries indicated by a current value of a read pointer; reading the contents of the second one of the plurality of entries into the transmit clock domain (col. 5, lines 18-25);

clearing the read valid bit associated with the second one of the plurality of entries (col. 5, lines 26-52 where disabling the reading of data is the equivalent to clearing the read valid bit because it stops the read operation); and

clearing a write valid bit associated with the second one of the plurality of entries (col. 7, lines 11-22 where disabling the writing of data is the equivalent to clearing the write valid bit because it stops the write operation)."

Regarding claim 6, New discloses, "the method of claim 5, further comprising: after the storing step, incrementing the write pointer (col. 4, lines 46-48)."

Regarding claim 7, New discloses, "the method of claim 6, further comprising: after the reading step, incrementing the read pointer (col. 7, lines 16-17)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over New (U.S. Patent 5,956,748).

Regarding claim 1, New discloses, "an interface circuit for communicating received data from a receive clock domain into a transmit clock domain, comprising:

a buffer, comprising a plurality of entries, having an input coupled to receive data from the receive clock domain and having an output for presenting data into the transmit clock domain (figure 2, element 202); and

a plurality of valid logic circuits, each associated with a corresponding one of the plurality of entries of the buffer (figure 2, elements 241 and 240 act as valid logic circuits by enabling the read and write operations)...comprising:

a write valid latch for controlling the state of a valid line in the receive clock domain, the write valid latch having a set input coupled to receive a write request signal (figure 2, element 214 as described in col. 7, lines 13-16 where the data in the latch is used to control the state of the write valid line);

a read valid latch for controlling the state of a valid line in the transmit clock domain, the read valid latch having a reset input coupled to receive a read request signal (figure 2, element 212 with similar operation to the latch 214 as described in col. 7, lines 13-16);

reset logic for resetting the write valid latch responsive to the read request signal (figure 2, elements 207, 221, and 223 act together to reset the logic in the latch as read in col. 7, lines 11-22);

set logic for setting the read valid latch responsive to the write request signal (figure 2, elements 208, 222, and 224 act together to set the logic in the latch as read in col. 5, lines 26-47)."

However, New does not explicitly show that "each valid logic circuit" contains the write latch, read latch, reset logic, and set logic. Although New shows the valid logic

circuits on either side of the figure, it would have been obvious to one with ordinary skill in the art at the time of invention to have all of the components of elements 240 and 241 (i.e. the write latch, read latch, reset logic, and set logic) combined into a single unit as a matter of design choice. The layout and placement of components in a given system are motivated by designer preference and the desired outputs are equivalent.

Regarding claim 2, New discloses the circuit of claim 1. Although New does not explicitly disclose the valid logic circuit containing all components, New further discloses, "write pointer logic for maintaining a write pointer indicating one of the entries of the buffer into which a next received data word is to be written from the receive clock domain (figure 2, element 205); and read pointer logic for maintaining a read pointer indicating one of the entries of the buffer from which a next data word is to be read into the transmit clock domain (figure 2, element 206)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the pointers with the circuit of claim 1 for the same reasons and motivation as in claim 1.

Regarding claim 3, New discloses the circuit of claim 1. Although New does not explicitly disclose the valid logic circuit containing all components, New further discloses, "a first edge detector circuit, for detecting a transition of the read request signal in the transmit clock domain (figure 2, element 207 as described in col. 5, lines 26-30 where 207 functions similarly to that of element 208 and where the comparator detects an edge by the comparison of the two signals, i.e. when one signal transitions

and is determined to be the same as the other, edge detection has occurred due to the transition); a first synchronizer circuit, having an input coupled to the first edge detector circuit, for generating, at an output coupled to a reset input of the write valid latch, a reset signal synchronized into the receive clock domain (figure 2, element 210)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the edge detector and synchronizer with the circuit of claim 1 for the same reasons and motivation as in claim 1.

Regarding claim 4, New discloses the circuit of claim 3. Although New does not explicitly disclose the valid logic circuit containing all components, New further discloses, "a second edge detector circuit, for detecting a transition of the write request signal in the receive clock domain (figure 2, element 208 as described in col. 5, lines 26-30 where the comparator detects an edge by the comparison of the two signals, i.e. when one signal transitions and is determined to be the same as the other, edge detection has occurred due to the transition); a second synchronizer circuit, having an input coupled to the second edge detector circuit, for generating, at an output coupled to a set input of the read valid latch, a set signal synchronized into the transmit clock domain (figure 2, element 210 where although there is a single synch circuit, one of ordinary skill in the art would recognize that one or two synch circuits is a matter of design choice)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the second edge detector with the second sync circuit with the circuit of claim 3 for the same reasons and motivation as in claim 3.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over New in view of Finney et al. (U.S. Patent 5,487,092).

Regarding claim 9, New discloses the method of claim 7. However, New lacks what Finney discloses, "responsive to the read valid bit associated with a second one of the plurality of entries indicating that the second one of the plurality of entries does not contain valid data, issuing an idle symbol (col. 7, lines 13-21 where the RN bits are the read valid bits causing the pad word or idle symbol to be inserted into the data stream; it should be noted that although New and Finney have obvious differences, what is being taken from Finney is the idea of inserting an idle symbol into the data, the differences between New and Finney with regard to the inserting of the idle symbol are irrelevant)."

It would have been obvious to one of ordinary skill in the art at the time of invention to include the inserting of the idle symbol for the purpose of providing for the "necessary flow control." The motivation for inserting the idle symbol is to effectively aid in synchronizing data flow between two different frequencies (or clocks).

Claims 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowe et al. (U.S. Patent 6,233,221 B1) in view of New.

Regarding claim 10, Lowe discloses, "a switch system for a communications network, comprising:

a plurality of switches, each having an interface for connecting to one or more network elements; a plurality of switch fabric devices, each comprising: a plurality of switch interfaces, each coupled to an associated one of the plurality of switches (figure 2, elements 205 and 209 where it is commonly known in the art that switch fabrics contain a plurality of switches to operate on a plurality of data inputs);

a first receive ring interface, operating in a receive clock domain (figure 1 shows how the network element of figure 2 is incorporated into a ring network, figure 2 shows element 204 acting as a first receive ring interface);

a first transmit ring interface, operating in a transmit clock domain (figure 2, element 202 is a first transmit ring interface and it is well known that communication networks operate in clock domains)...

a first ring path, having an input coupled to the first ring receive interface and having an output (figure 1, where the inside ring is the first ring path)...

a second receive ring interface (figure 1, where each network element has a receive ring interface as described in figure 2, therefore there is at least a second receive ring interface in the network);

a second ring path, having an input coupled to the second ring receive interface and having an output (figure 1, where the outside ring is the second ring path);

a second transmit ring interface (figure 1, where each network element has a transmit ring interface as described in figure 2, therefore there is at least a second transmit ring interface in the network);

wherein the first receive ring interface and the second transmit ring interface correspond to a first ring interface that is coupled to a ring interface of another one of the plurality of switch fabric devices, and wherein the first transmit ring interface and the second receive ring interface correspond to a second ring interface that is coupled to a ring interface of another one of the plurality of switch fabric devices, such that the plurality of switch fabric devices are interconnected into a ring (figure 1 shows that each network element is connected through each of their respective interfaces and as pictured are arranged into a ring structure)."

However, Lowe lacks what New discloses, that is "a transmit clock generator circuit, for generating a clock signal for controlling the operation of the first transmit ring interface (figure 2 where if a clock signal exists in the system, it must have been generated by a device); and

a buffer, comprising a plurality of entries, having an input coupled to receive data from the receive clock domain and having an output for presenting data into the transmit clock domain (figure 2, element 202); and

a plurality of valid logic circuits, each associated with a corresponding one of the plurality of entries of the buffer (figure 2, elements 241 and 240 act as valid logic circuits by enabling the read and write operations)...comprising:

a write valid latch for controlling the state of a valid line in the receive clock domain, the write valid latch having a set input coupled to receive a write request signal (figure 2, element 214 as described in col. 7, lines 13-16 where the data in the latch is used to control the state of the write valid line);

a read valid latch for controlling the state of a valid line in the transmit clock domain, the read valid latch having a reset input coupled to receive a read request signal (figure 2, element 212 with similar operation to the latch 214 as described in col. 7, lines 13-16);

reset logic for resetting the write valid latch responsive to the read request signal (figure 2, elements 207, 221, and 223 act together to reset the logic in the latch as read in col. 7, lines 11-22);

set logic for setting the read valid latch responsive to the write request signal (figure 2, elements 208, 222, and 224 act together to set the logic in the latch as read in col. 5, lines 26-47)."

However, New does not explicitly show that "each valid logic circuit" contains the write latch, read latch, reset logic, and set logic. Although New shows the valid logic circuits on either side of the figure, it would have been obvious to one with ordinary skill in the art at the time of invention to have all of the components of elements 240 and 241 (i.e. the write latch, read latch, reset logic, and set logic) combined into a single unit as a matter of design choice. The layout and placement of components in a given system are motivated by designer preference and the desired outputs are equivalent.

Regarding claim 15, Lowe and New disclose the system of claim 10. However, Lowe lacks what New further discloses, "wherein the reset logic comprises: a first edge detector circuit, for detecting a transition of the read request signal in the transmit clock domain (figure 2, element 207 as described in col. 5, lines 26-30 where 207 functions

similarly to that of element 208 and where the comparator detects an edge by the comparison of the two signals, i.e. when one signal transitions and is determined to be the same as the other, edge detection has occurred due to the transition); a first synchronizer circuit, having an input coupled to the first edge detector circuit, for generating, at an output coupled to a reset input of the write valid latch, a reset signal synchronized into the receive clock domain (figure 2, element 210);

and wherein the set logic comprises:

a second edge detector circuit, for detecting a transition of the write request signal in the receive clock domain (figure 2, element 208 as described in col. 5, lines 26-30 where the comparator detects an edge by the comparison of the two signals, i.e. when one signal transitions and is determined to be the same as the other, edge detection has occurred due to the transition); a second synchronizer circuit, having an input coupled to the second edge detector circuit, for generating, at an output coupled to a set input of the read valid latch, a set signal synchronized into the transmit clock domain (figure 2, element 210 where although there is a single synch circuit, one of ordinary skill in the art would recognize that one or two synch circuits is a matter of design choice)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the edge detectors and synchronizers with the system of claim 10 for the same reasons and motivation as in claim 10.

Allowable Subject Matter

Claims 8 and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 2 September 2004 have been fully considered but they are not persuasive. Applicant states that amended drawings have been filed, but there are no such amended drawings. Therefore, the objection to the drawings is maintained.

Applicant's arguments, see REMARKS, page 8, Claim Objections, filed 2 September 2004, with respect to the claim objections have been fully considered and are persuasive. The objections of claims 8, 10, and 14 have been withdrawn.

Applicant's arguments, see REMARKS, page 8, Rejection of Claims under 35 U.S.C. 103, filed 2 September 2004, with respect to the rejection(s)of claim(s) 1, 2, 3-13, and 15 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art and a better understanding of applicant's invention (claims 1-7, 9, 10, and 15 only).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Kading whose telephone number is (571) 272-3070. The examiner can normally be reached on M-F: 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joshua Kading
Examiner
Art Unit 2661

January 5, 2005

BOB PHUNKULH
PRIMARY EXAMINER